PATENT & TRADEMARK OFFICE
MAR 01 2004
OIPE
JC42

FIG. 1A

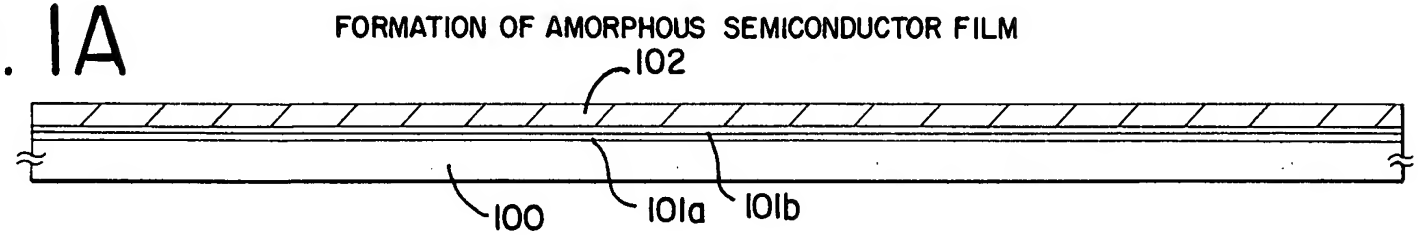


FIG. 1B

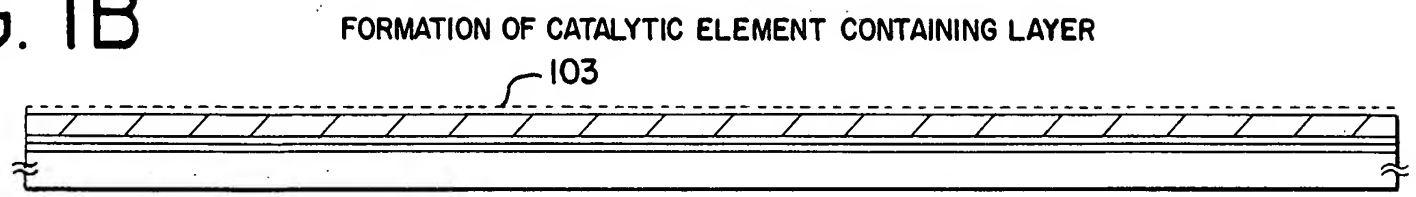


FIG. 1C

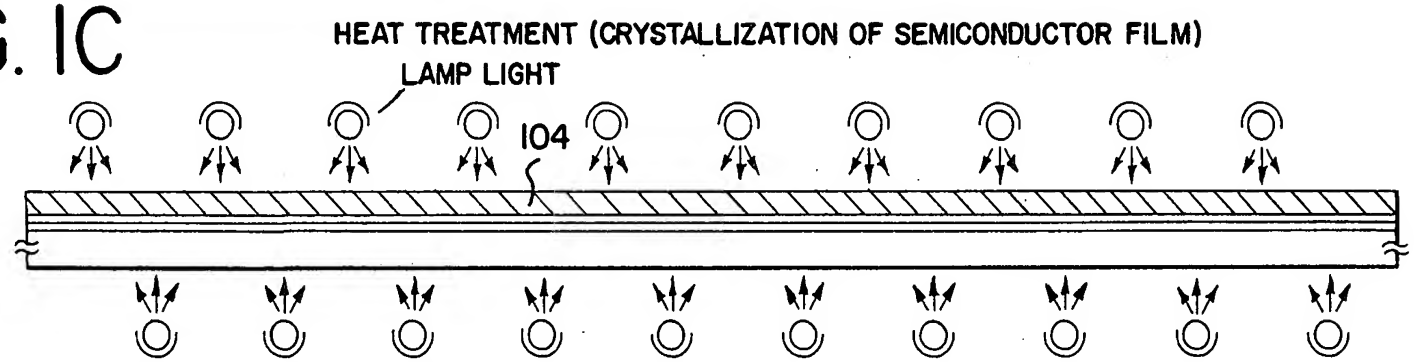
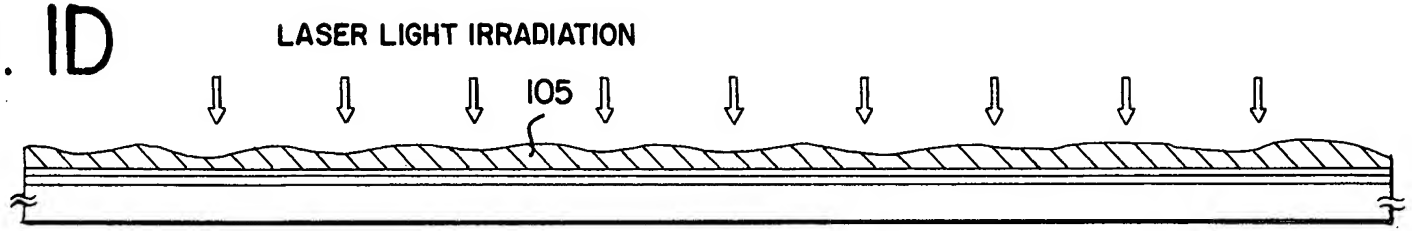


FIG. 1D



PATENT & TRADEMARK OFFICE
MAR 01 2004
OIPE
JC42

FIG. 2A

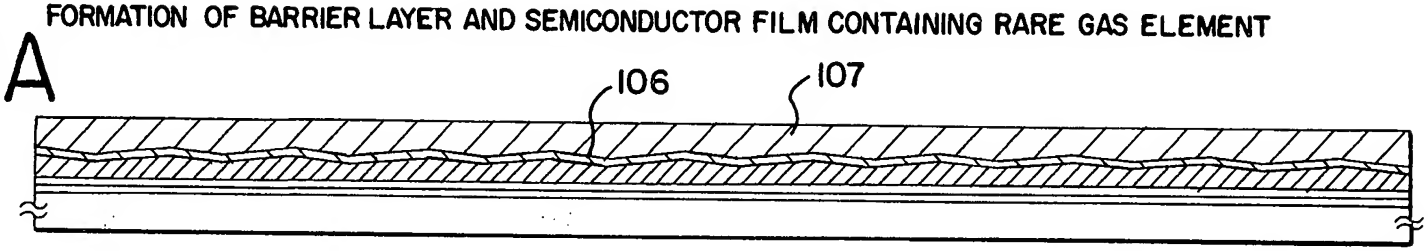


FIG. 2B

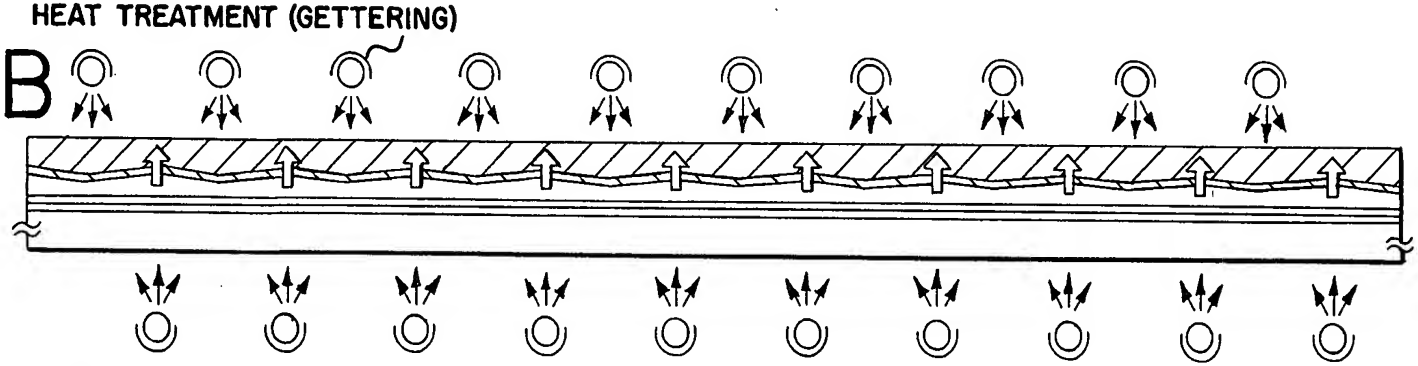


FIG. 2C

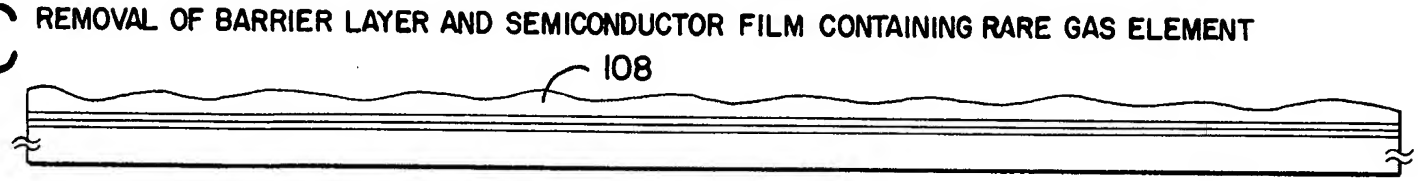
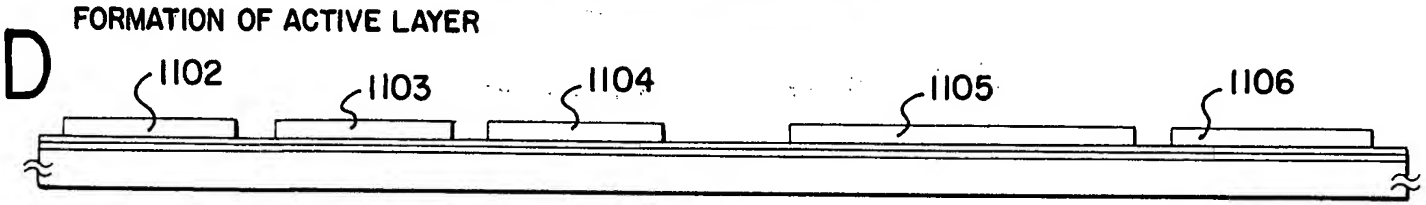


FIG. 2D



PATENT & TRADEMARK OFFICE
MAR 01 2004
JC42
O I P E

FIG. 3A

FORMATION OF SEMICONDUCTOR LAYER/FORMATION OF INSULATING FILM/
FORMATION OF FIRST CONDUCTIVE FILM AND SECOND CONDUCTIVE FILM

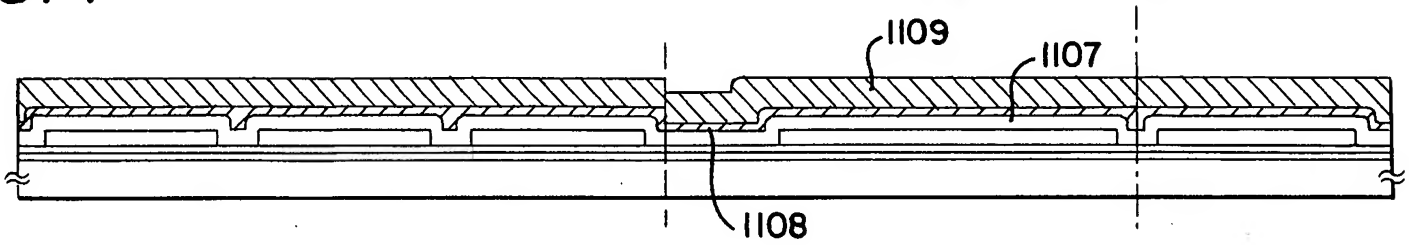


FIG. 3B

FIRST ETCHING PROCESS

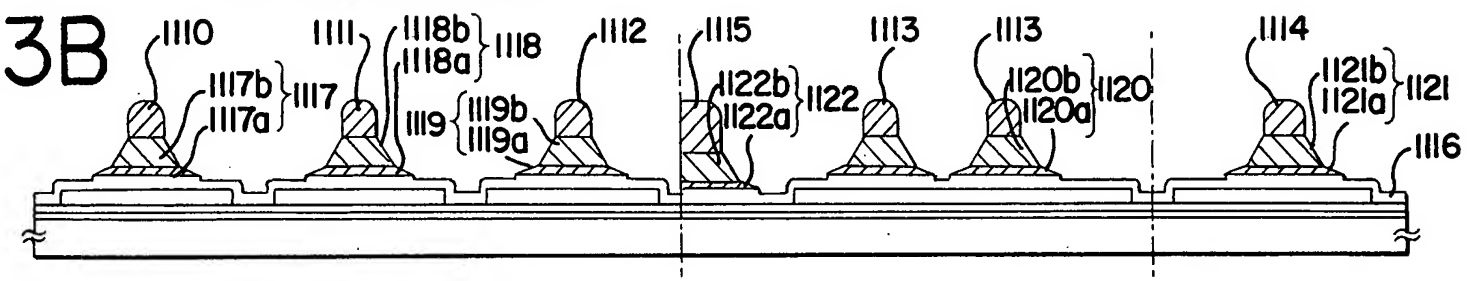
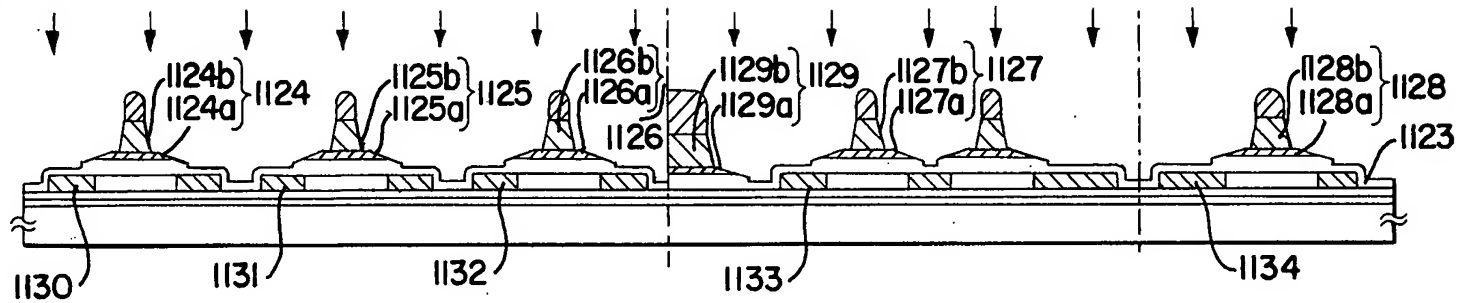


FIG. 3C

SECOND ETCHING PROCESS/
FIRST DOPING PROCESS



PATENT & TRADEMARK OFFICE
MAR 01 2004
O I P E
JC42

FIG. 4A

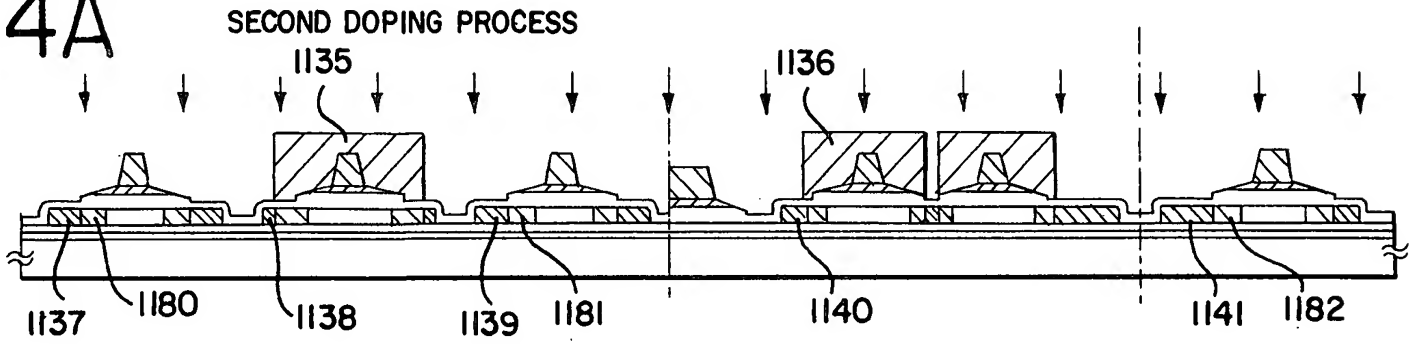


FIG. 4B

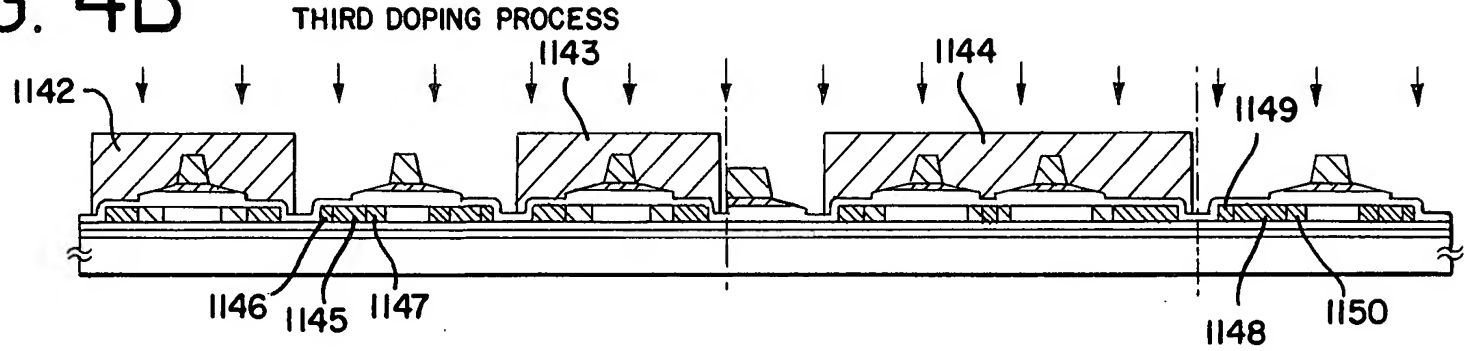
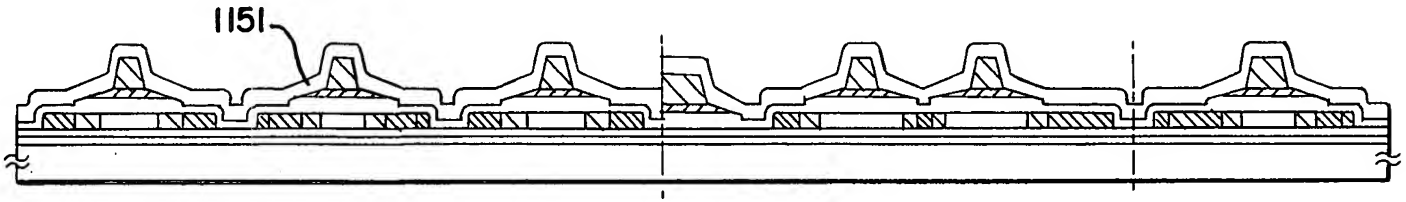


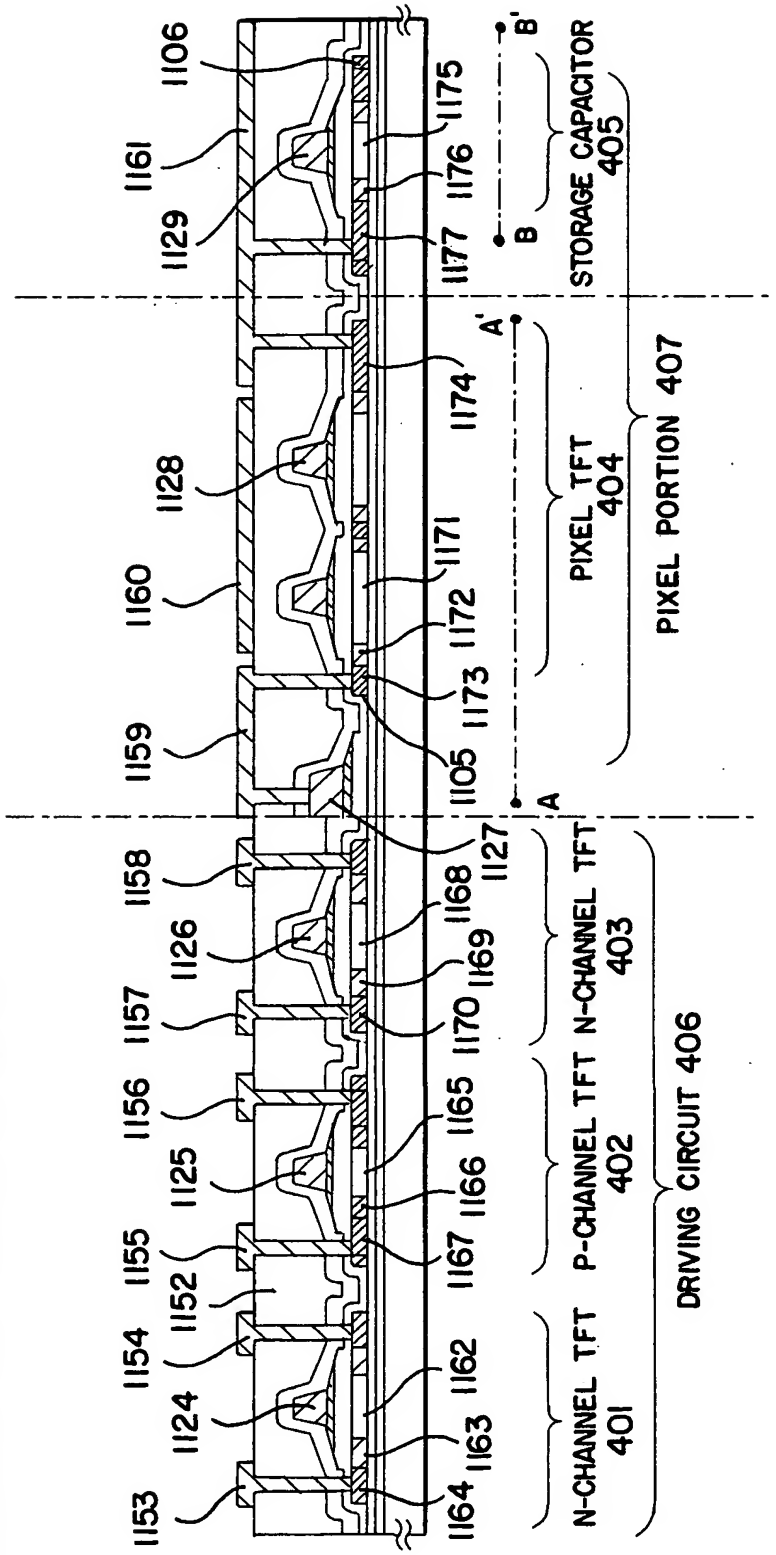
FIG. 4C



OIPE JC42
MAR 01 2004
PATENT & TRADEMARK OFFICE

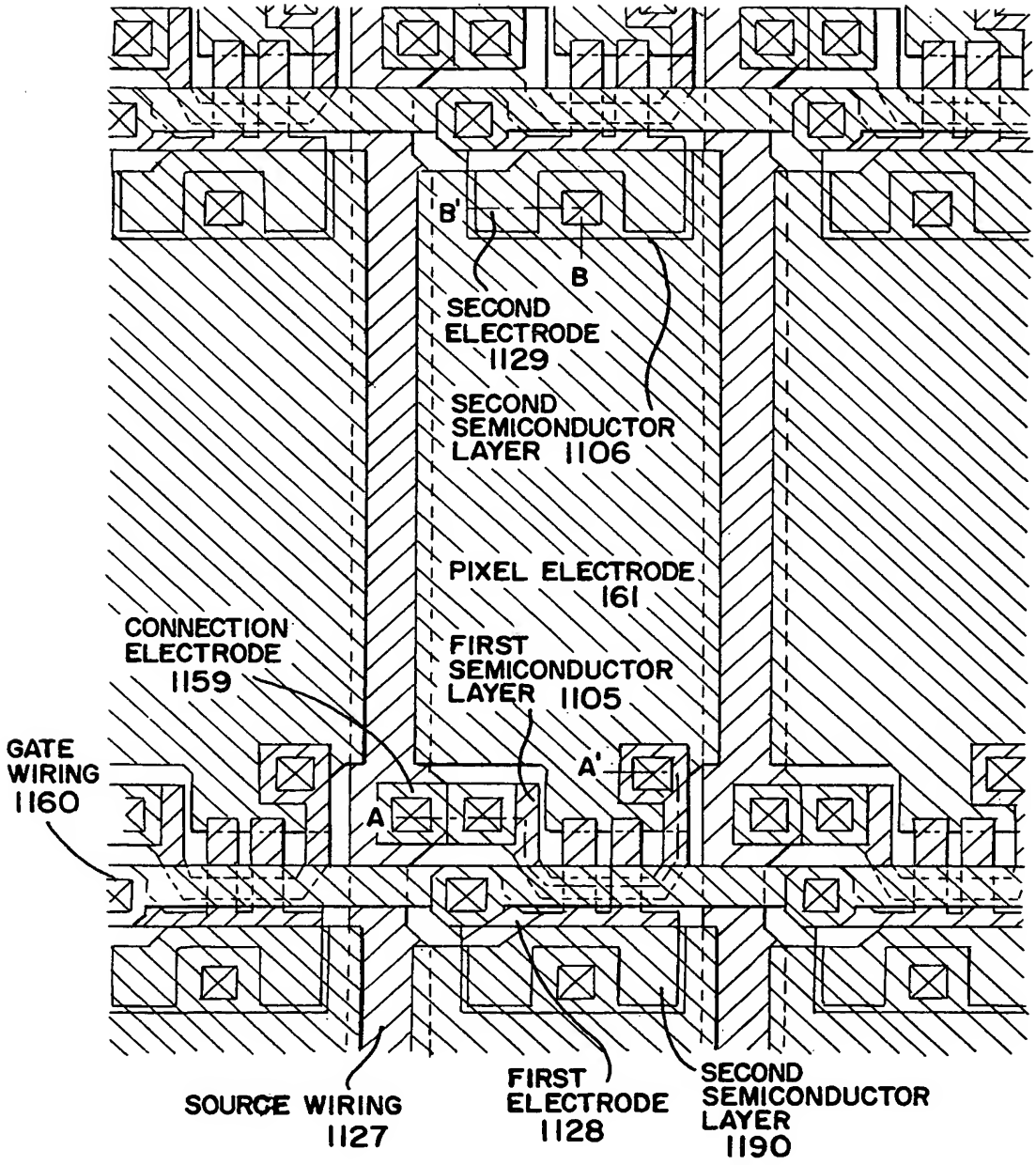
FIG. 5

FORMATION OF INTERPLAYER INSULATING FILM
FORMATION OF PIXEL ELECTRODE AND WIRING



O I P E
MAR 0 1 2004
PATENT & TRADEMARK OFFICE
JC42

FIG. 6



O I P E
MAR 0 1 2004
JC42
PATENT & TRADEMARK OFFICE

FIG. 7A

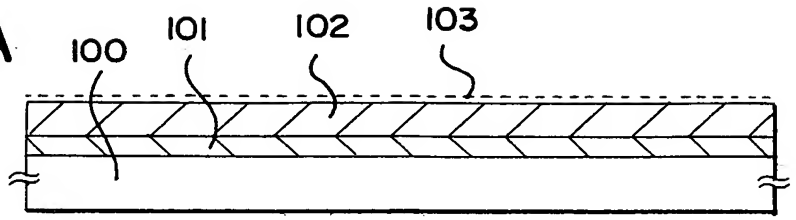


FIG. 7B

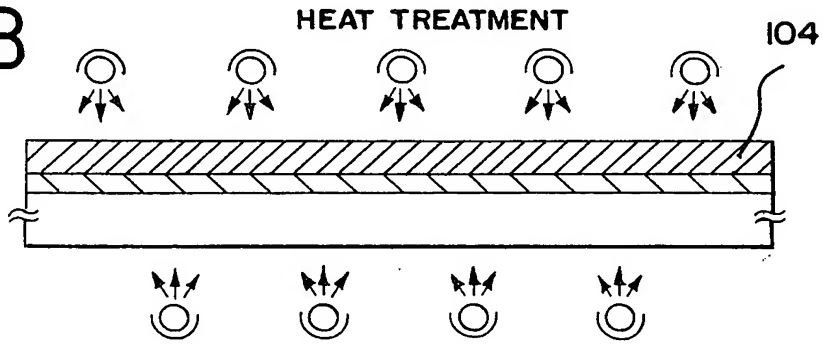


FIG. 7C

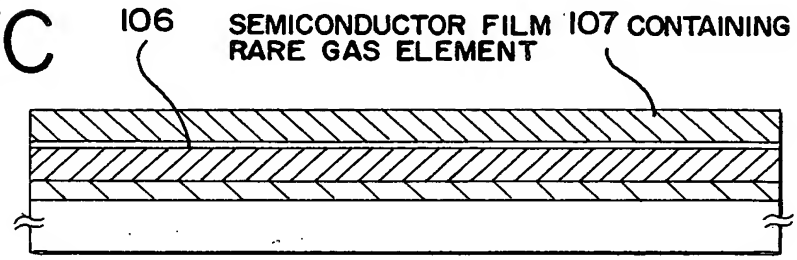


FIG. 7D

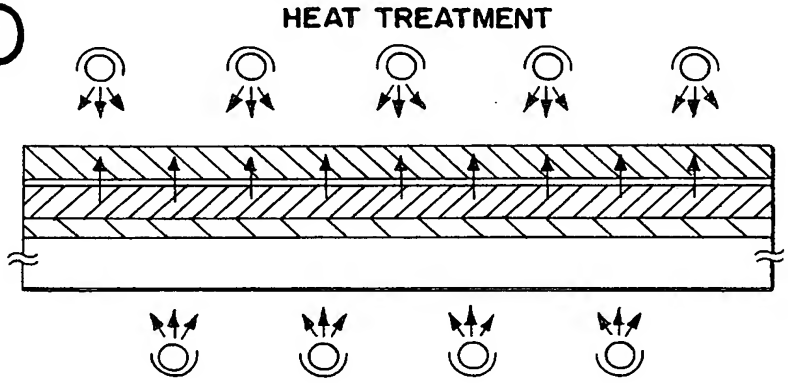
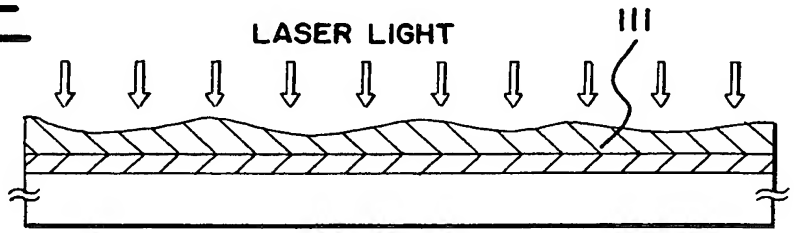


FIG. 7E



O I P E
MAR 0 1 2004
PATENT & TRADEMARK OFFICE

FIG. 8A

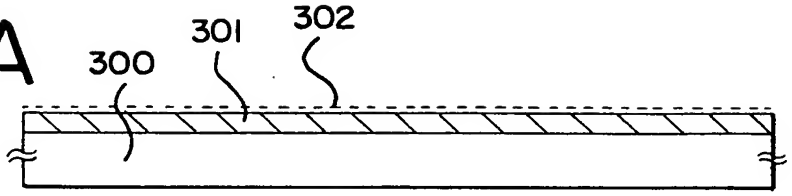


FIG. 8B

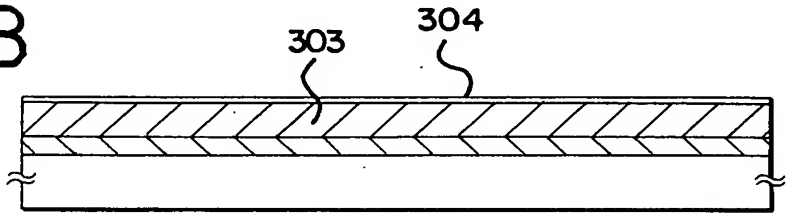


FIG. 8C

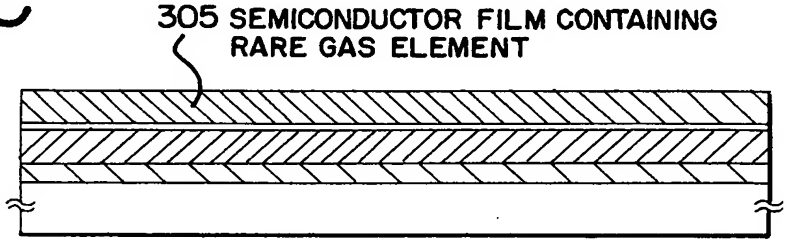


FIG. 8D

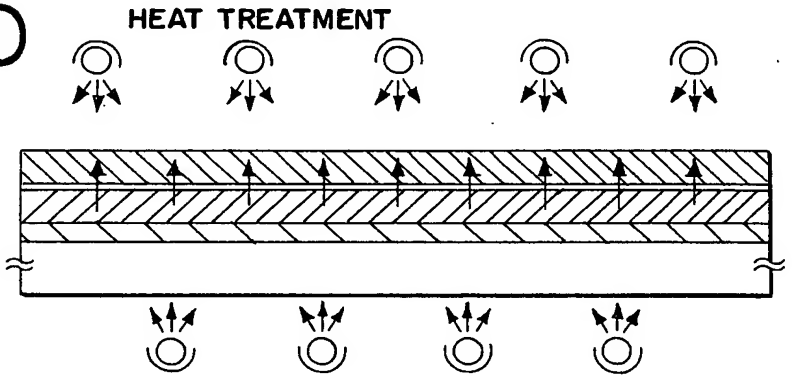
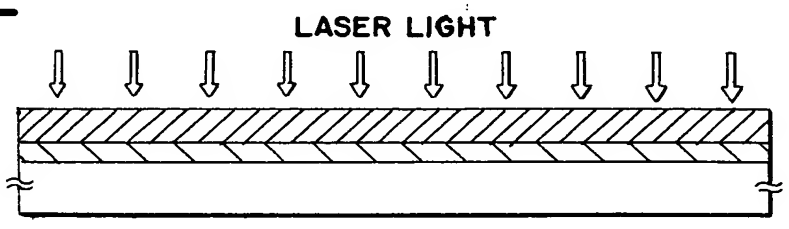
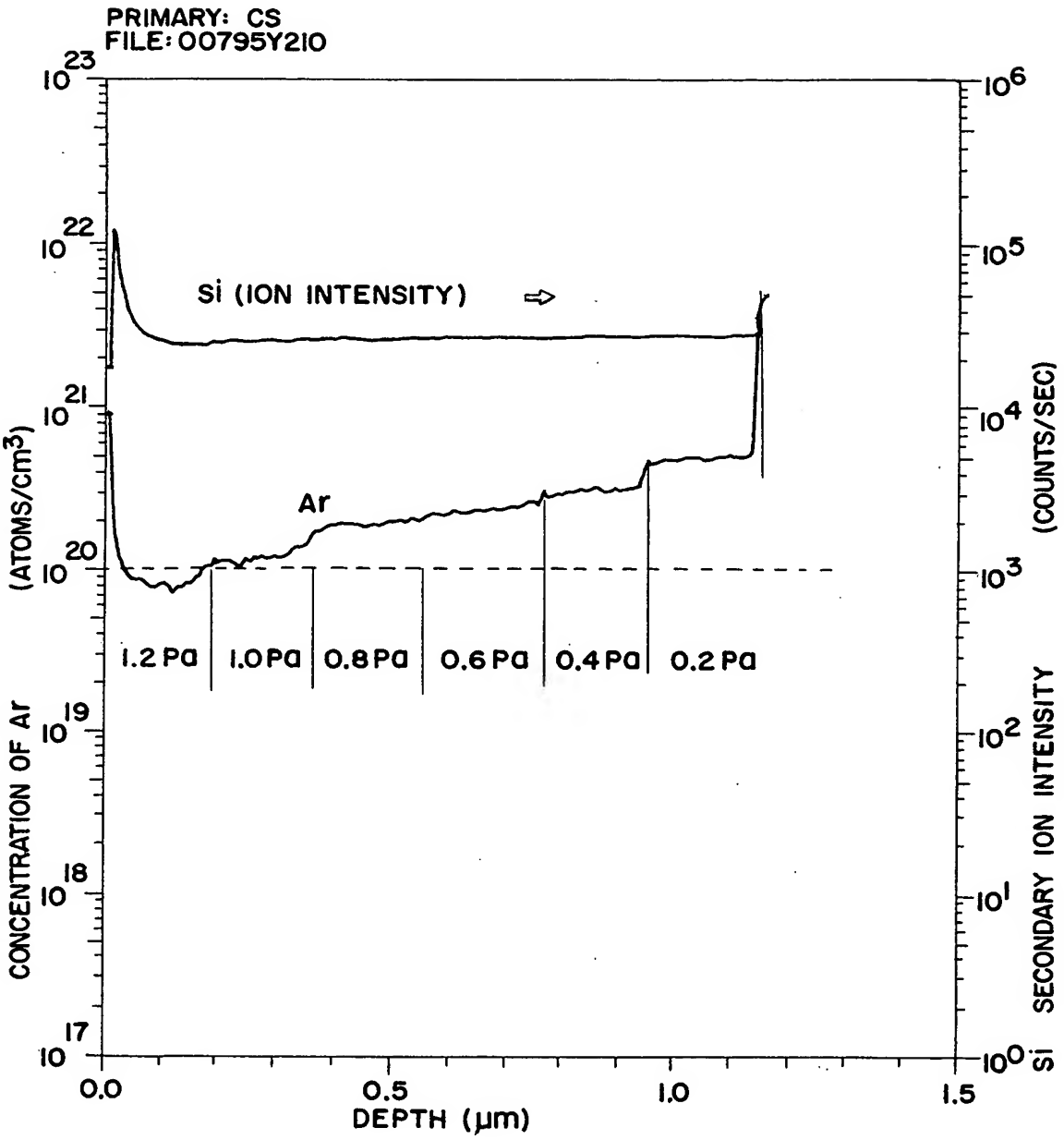


FIG. 8E



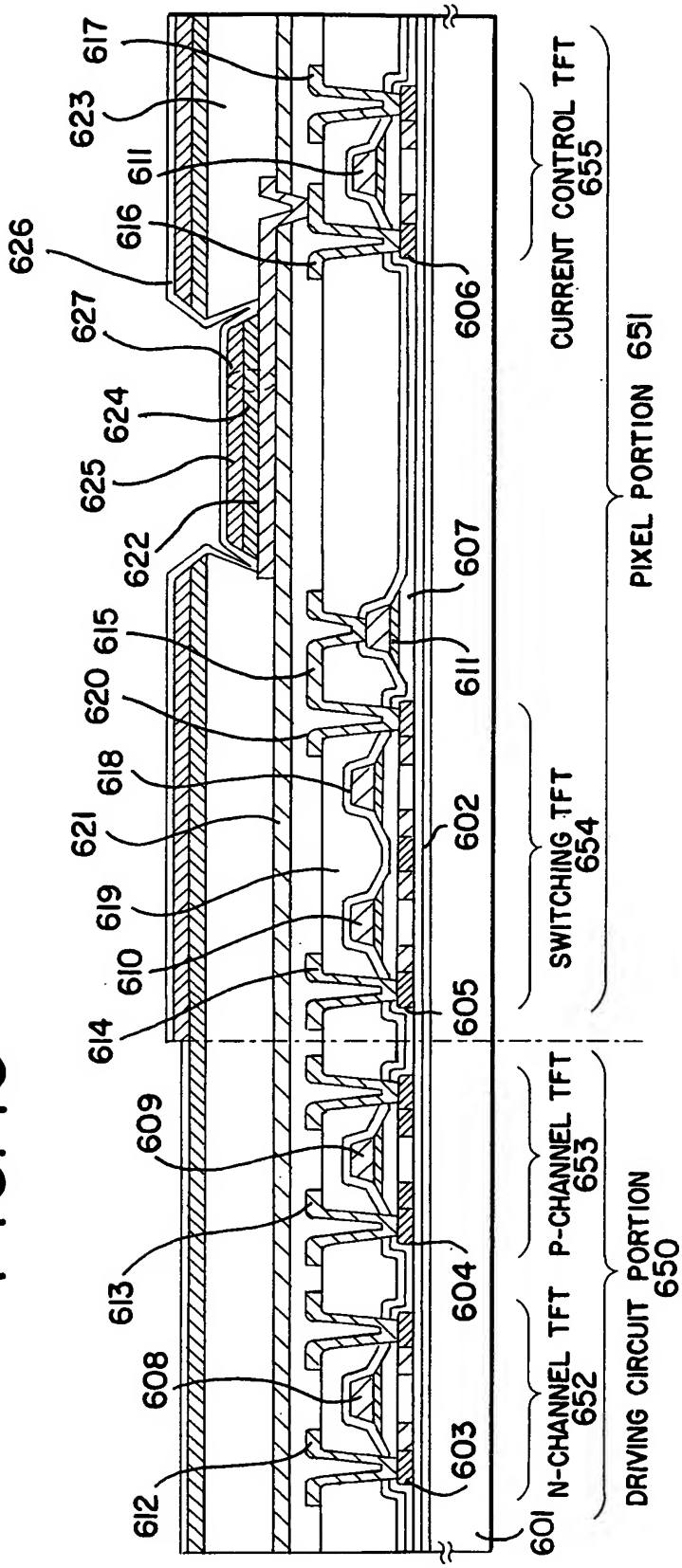
O I P E
MAR 0 1 2004
PATENT & TRADEMARK OFFICE
JC42

FIG. 9



O I P E
MAR 0 1 2004
PATENT & TRADEMARK OFFICE
JC42

FIG. 10



OIPE
MAR 0 1 2004
PATENT & TRADEMARK OFFICE

FIG. 11A

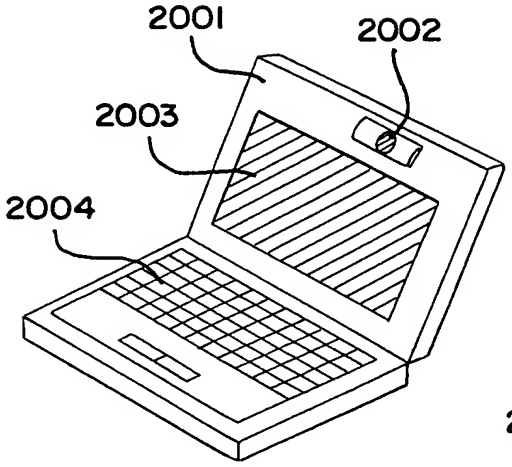


FIG. 11B

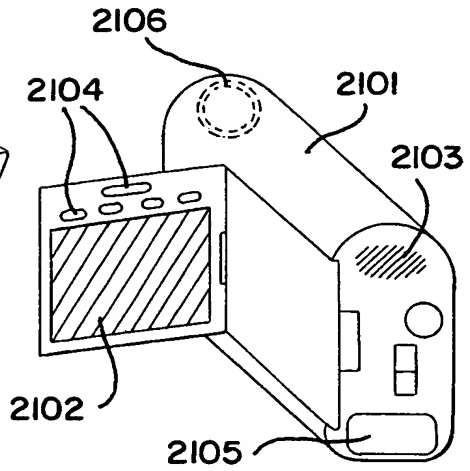


FIG. 11C

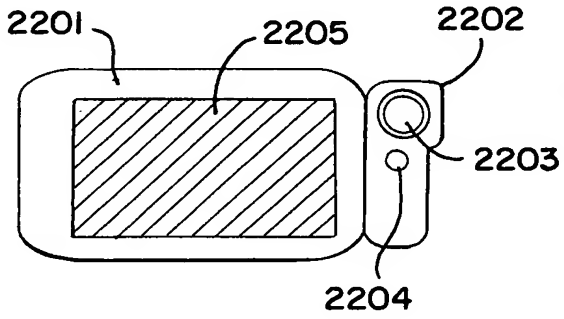


FIG. 11D

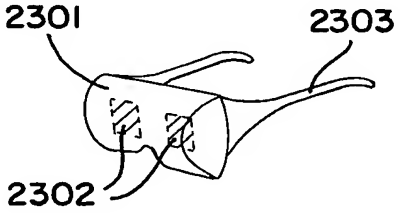


FIG. 11E

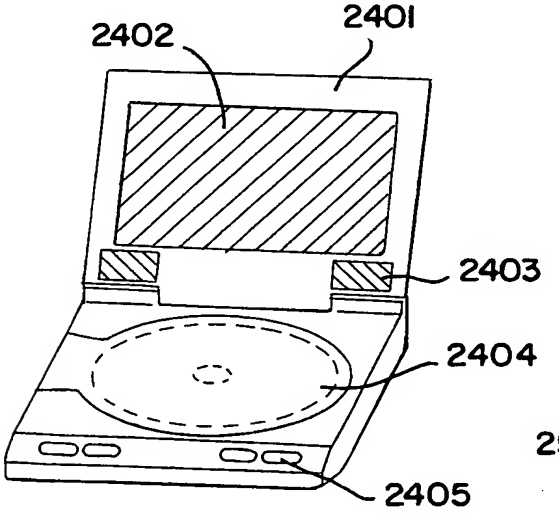
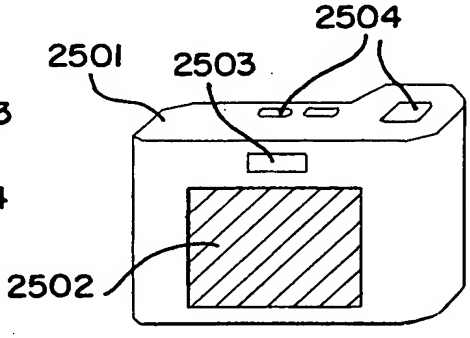


FIG. 11F



O I P E
MAR 0 1 2004
PATENT & TRADEMARK OFFICE
JC42

FIG. 12A

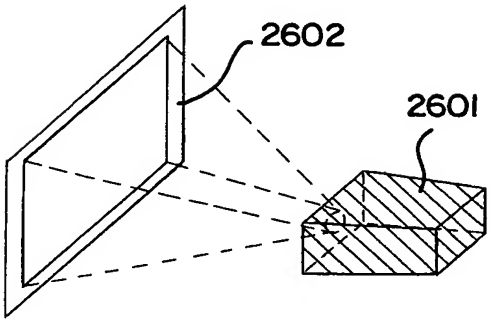


FIG. 12B

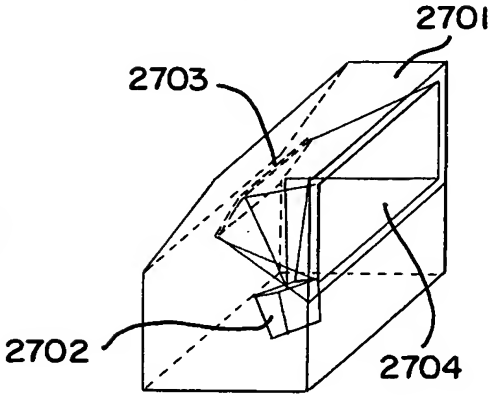


FIG. 12C

PROJECTION APPARATUS
(THREE PLATES TYPE)

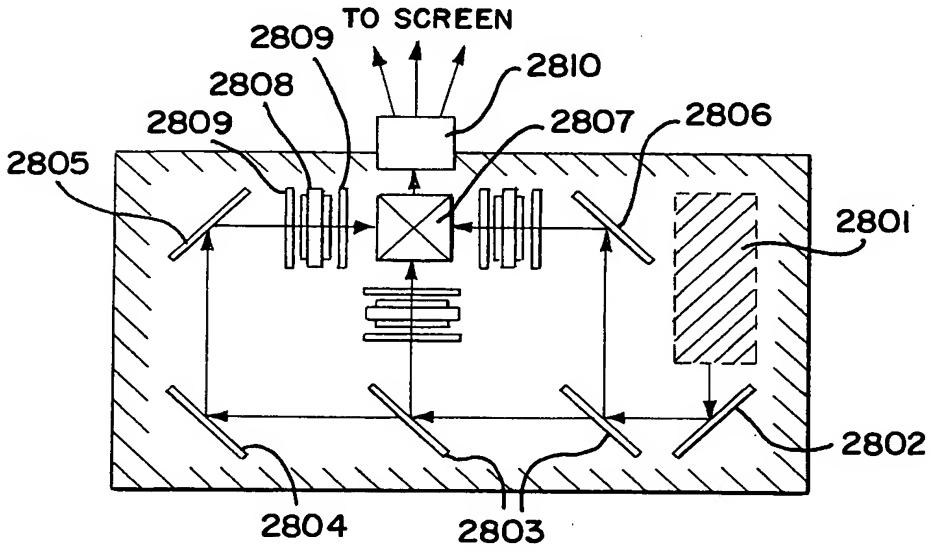
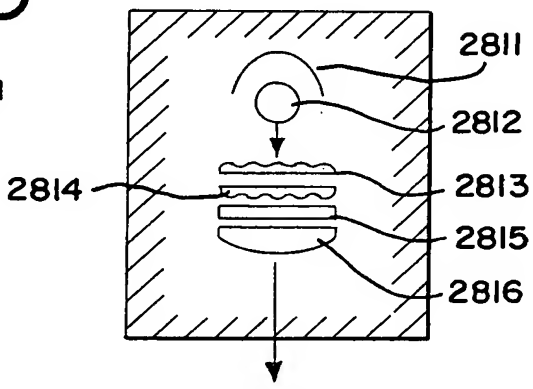


FIG. 12D

LIGHT SOURCE
OPTICAL SYSTEM



O I P E
MAR 0 1 2004
PATENT & TRADEMARK OFFICE
JC42

FIG. 13A

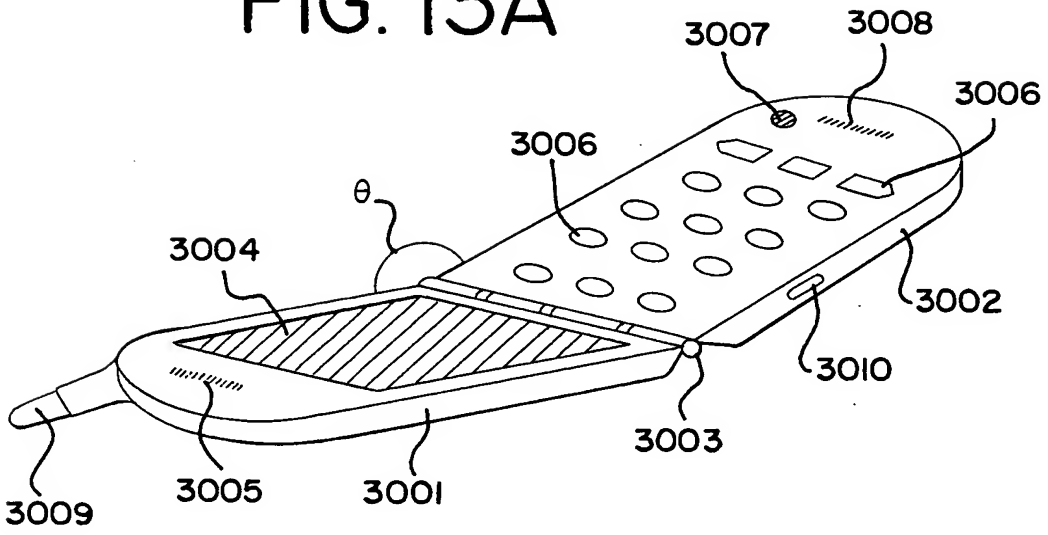


FIG. 13B

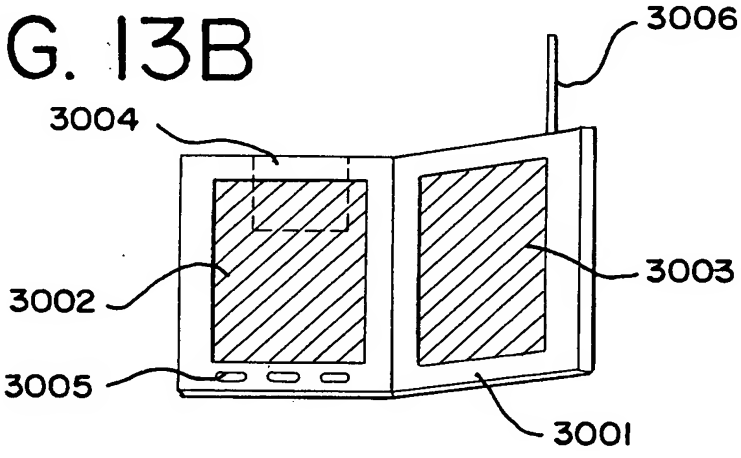
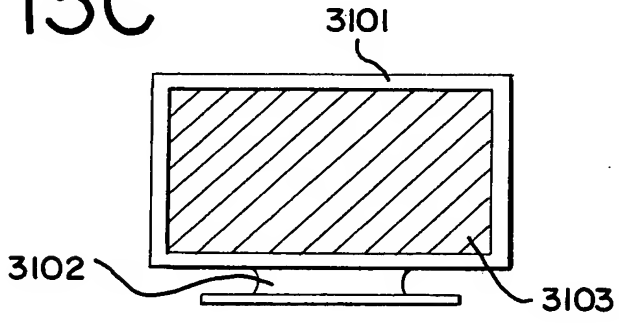


FIG. 13C



O I P E
MAR 0 1 2004
PATENT & TRADEMARK OFFICE
JC42

FIG. 14A

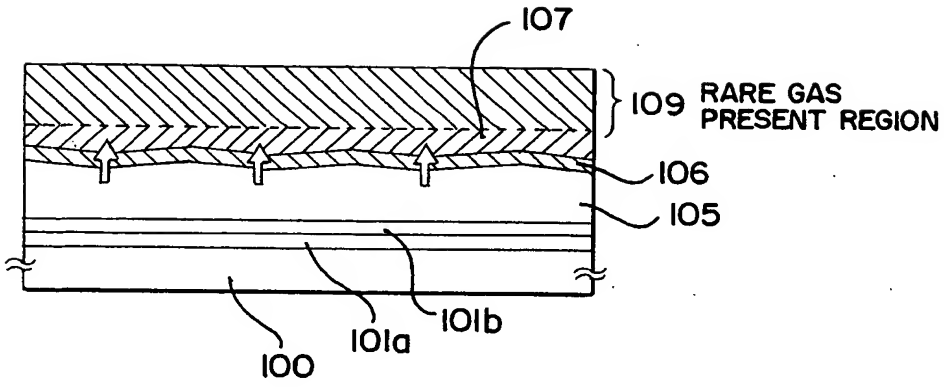


FIG. 14B

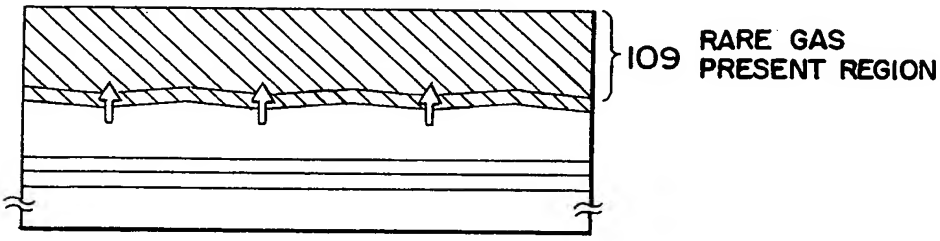
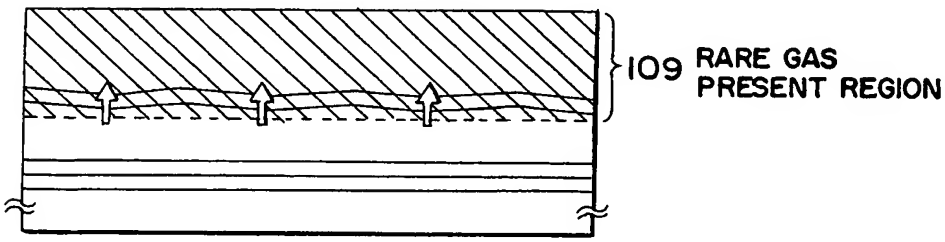


FIG. 14C



OIPE
MAR 0 1 2004
PATENT & TRADEMARK OFFICE
JC42

FIG. 15A

FORMATION OF GATE WIRING

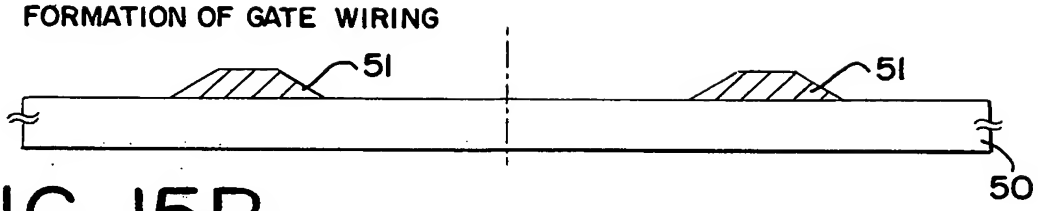


FIG. 15B

FORMATION OF GATE
INSULATING FILM
AND SEMICONDUCTOR FILM

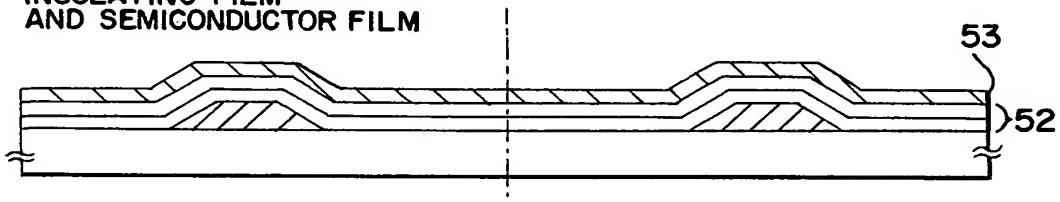


FIG. 15C

CRYSTALLIZATION

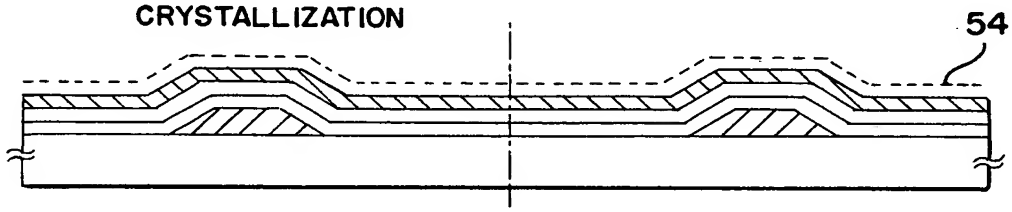


FIG. 15D

GETTERING

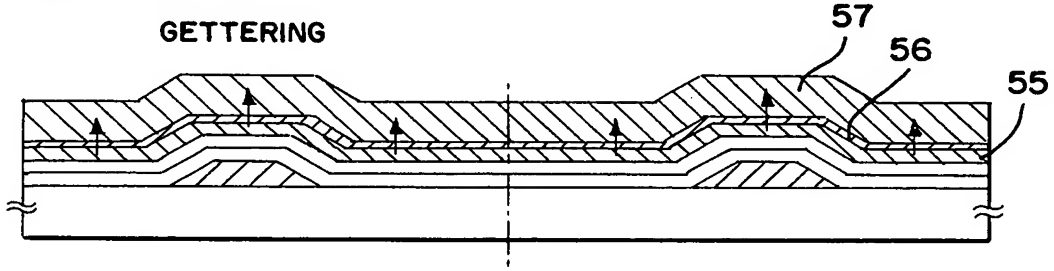
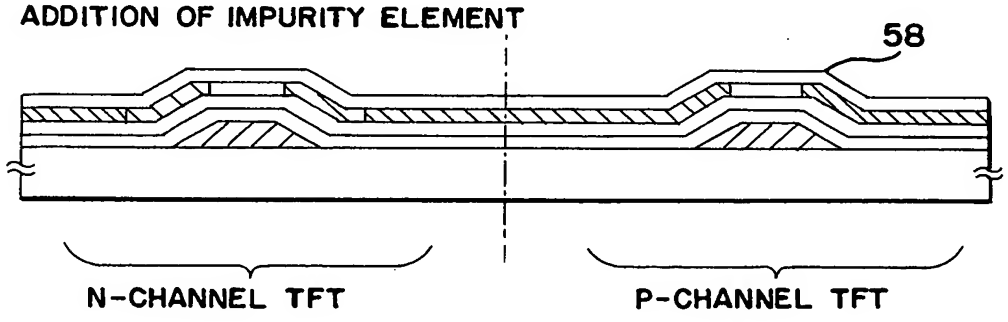


FIG. 15E

ADDITION OF IMPURITY ELEMENT



O-I P E
MAR 0 1 2004
PATENT & TRADEMARK OFFICE
JC42

FIG. 16A

ACTIVATION

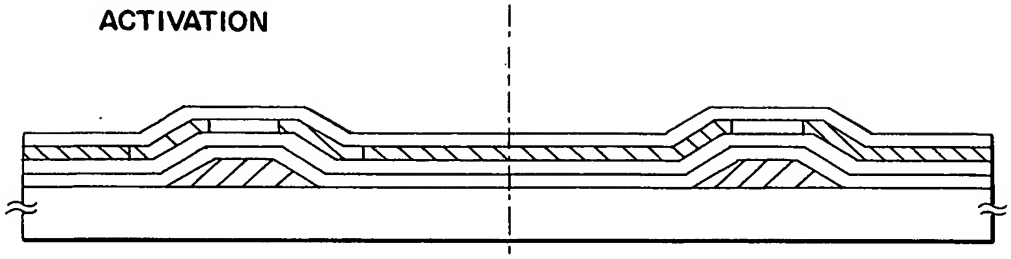


FIG. 16B

FORMATION OF INTERLAYER INSULATING FILM

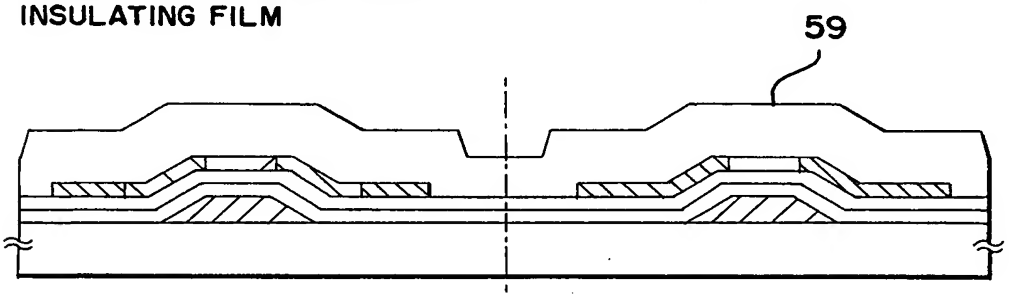
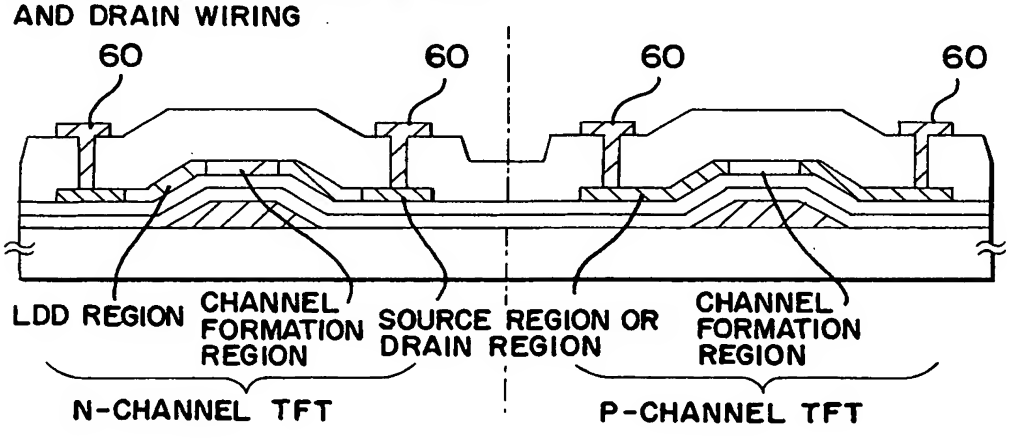


FIG. 16C

FORMATION OF SOURCE WIRING AND DRAIN WIRING



O I P E
MAR 0 1 2004
JC42
PATENT & TRADEMARK OFFICE

FIG. 17A

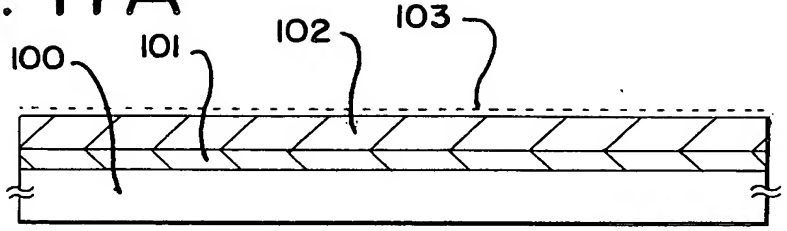


FIG. 17B

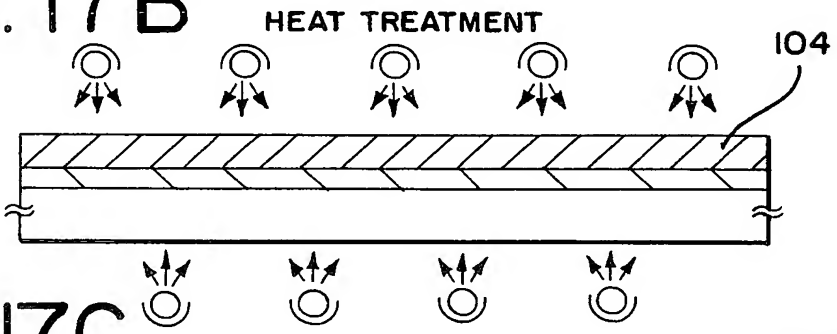


FIG. 17C

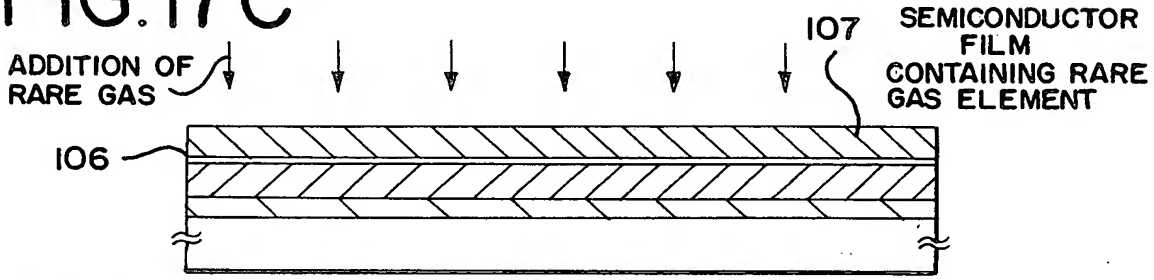


FIG. 17D

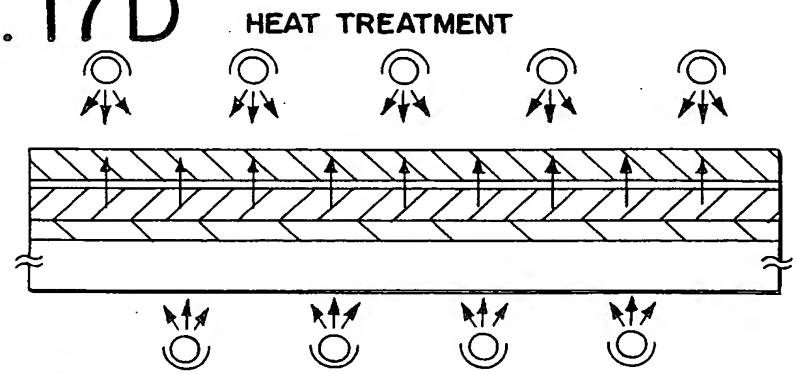
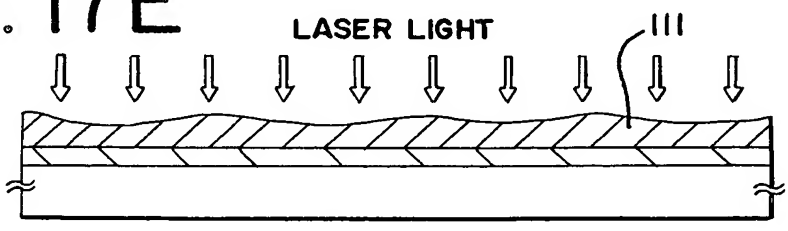
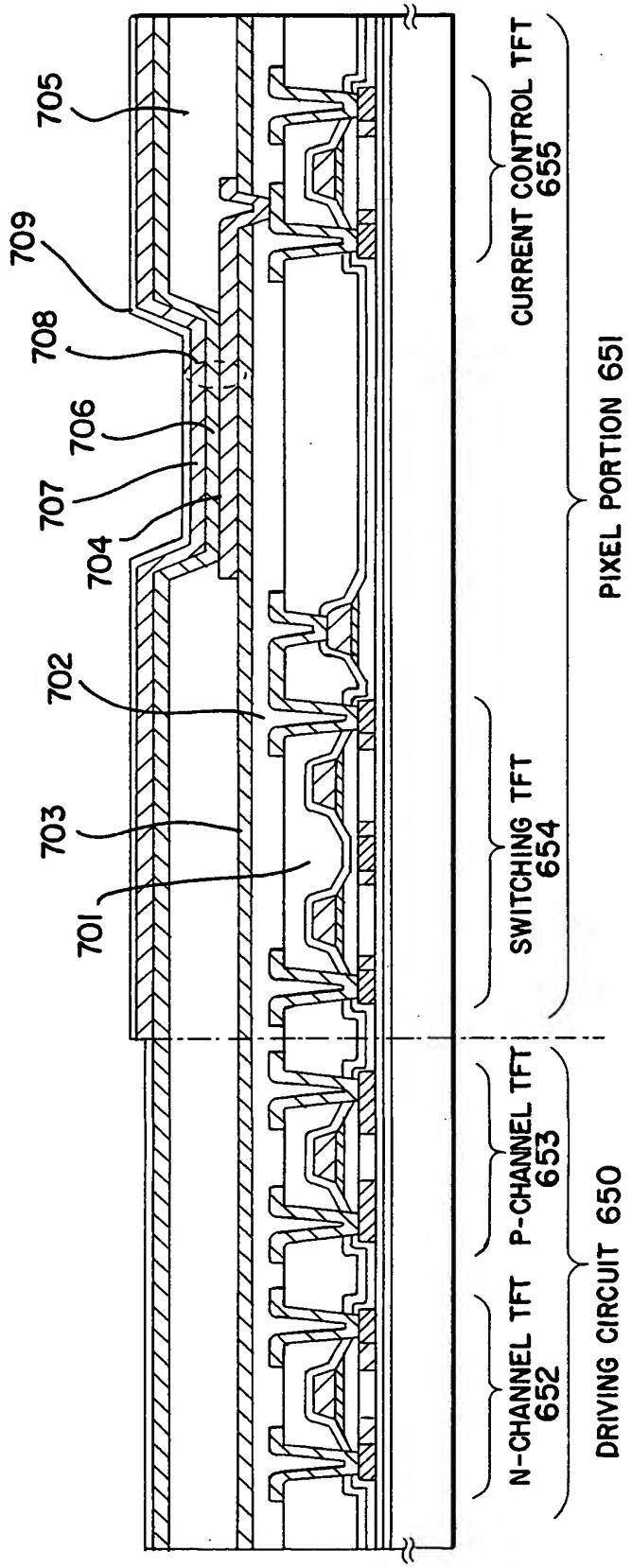


FIG. 17E



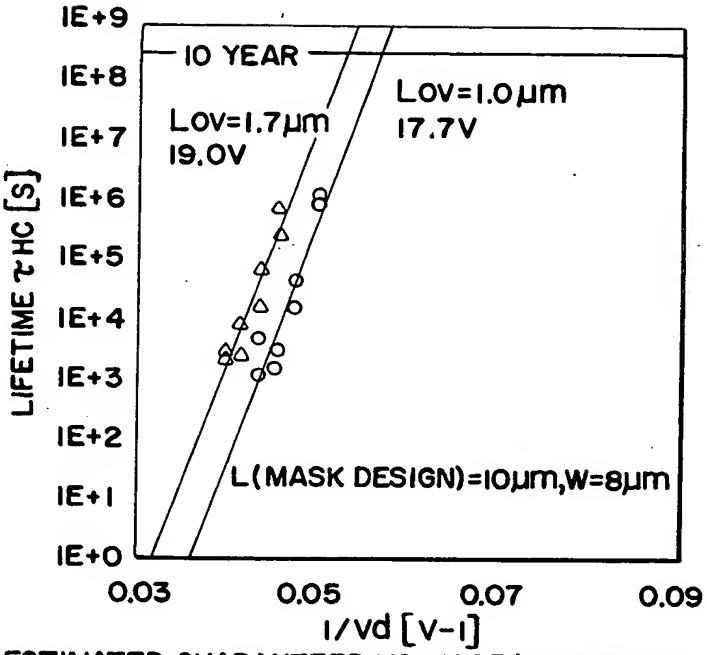
O I P E
MAR 0 1 2004
PATENT & TRADEMARK OFFICE
JC42

FIG. 18



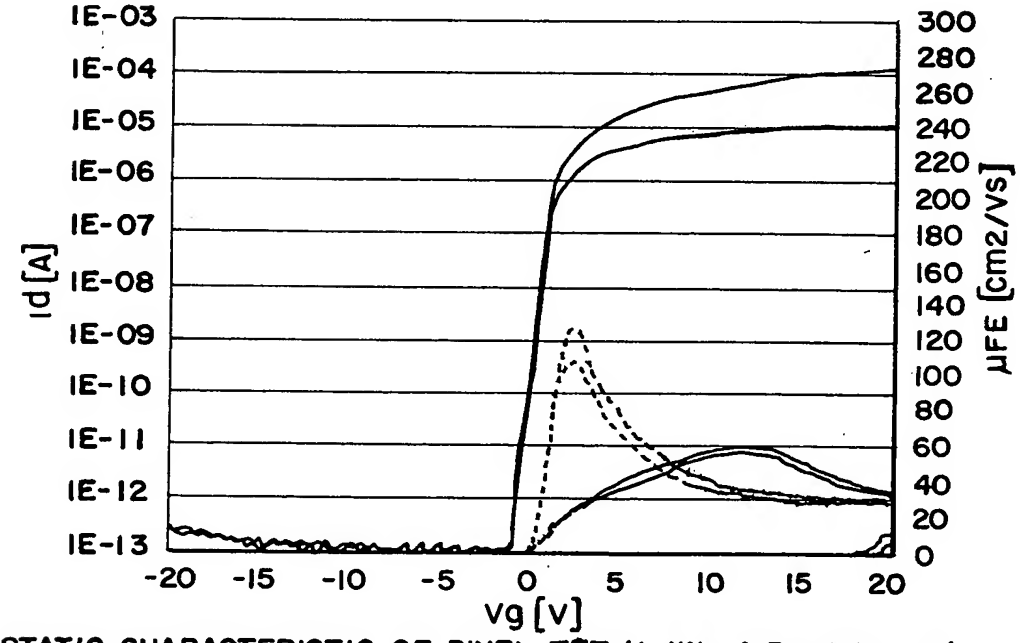
O I P E
MAR 0 1 2004
PATENT & TRADEMARK OFFICE
JC42

FIG. 19A



ESTIMATED GUARANTEED VOLTAGE (ON CURRENT 10% DEGRADATION) DEPENDENCE ON LENGTH OF LOV (L/W=10/8 μm)

FIG. 19B



STATIC CHARACTERISTIC OF PIXEL TFT (L/W=4.5 x 2/3 μm)